Understanding the Process of Writing Papers for MTT-S Publications

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Editor, IEEE Microwave and Wireless Components Letters (2006-2009)

Why Write Papers

Scientific Process

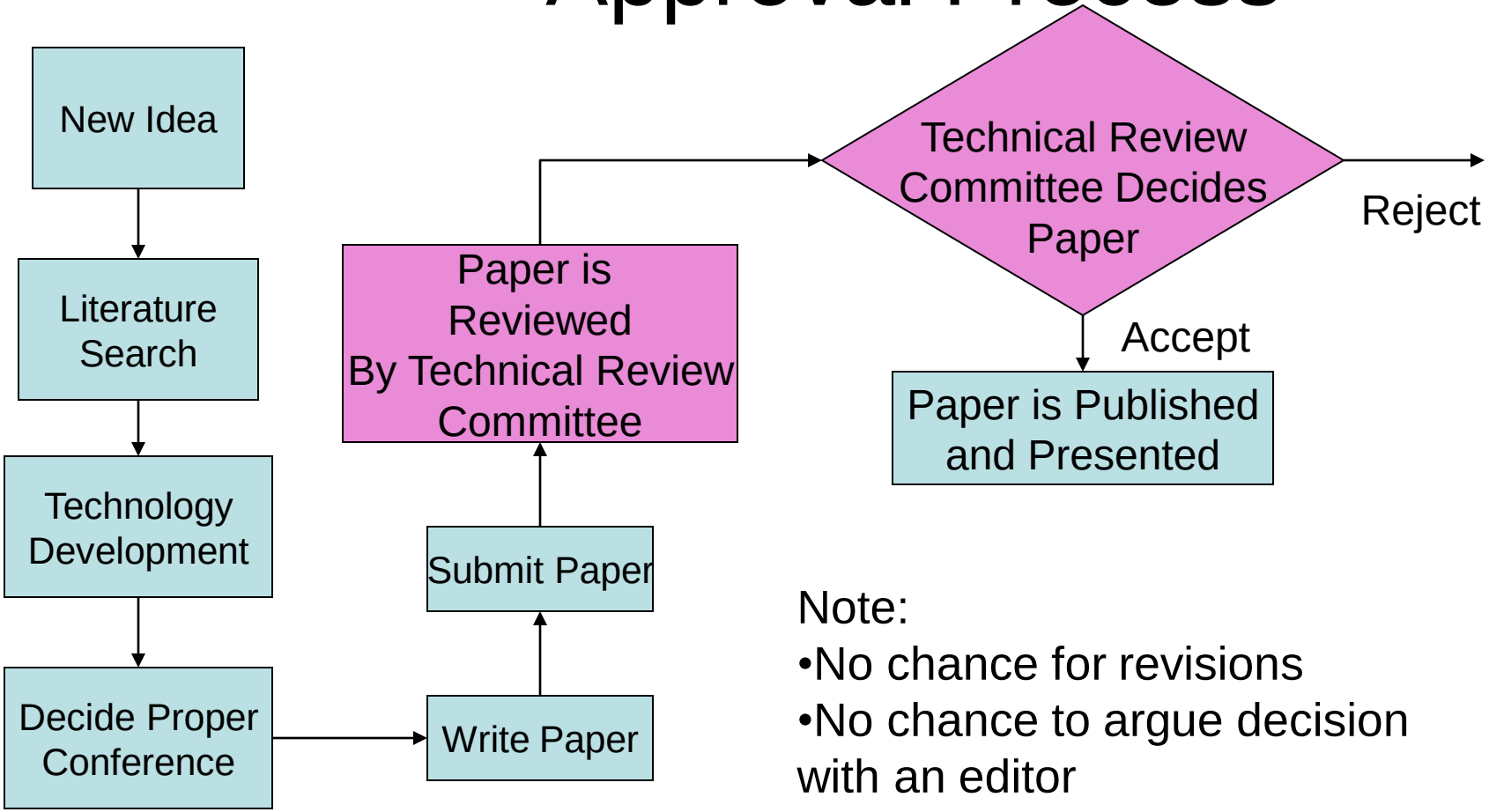
- Publish new scientific results
- Allow other researchers to confirm your results
- Allow other researchers to extend your results
- Clarify difficult concepts for the other engineers and the general public

Personal Reasons

- Establish priority (private notebooks do not establish your priority)
- Publicize (advertise) new technology capability
- Career advancement

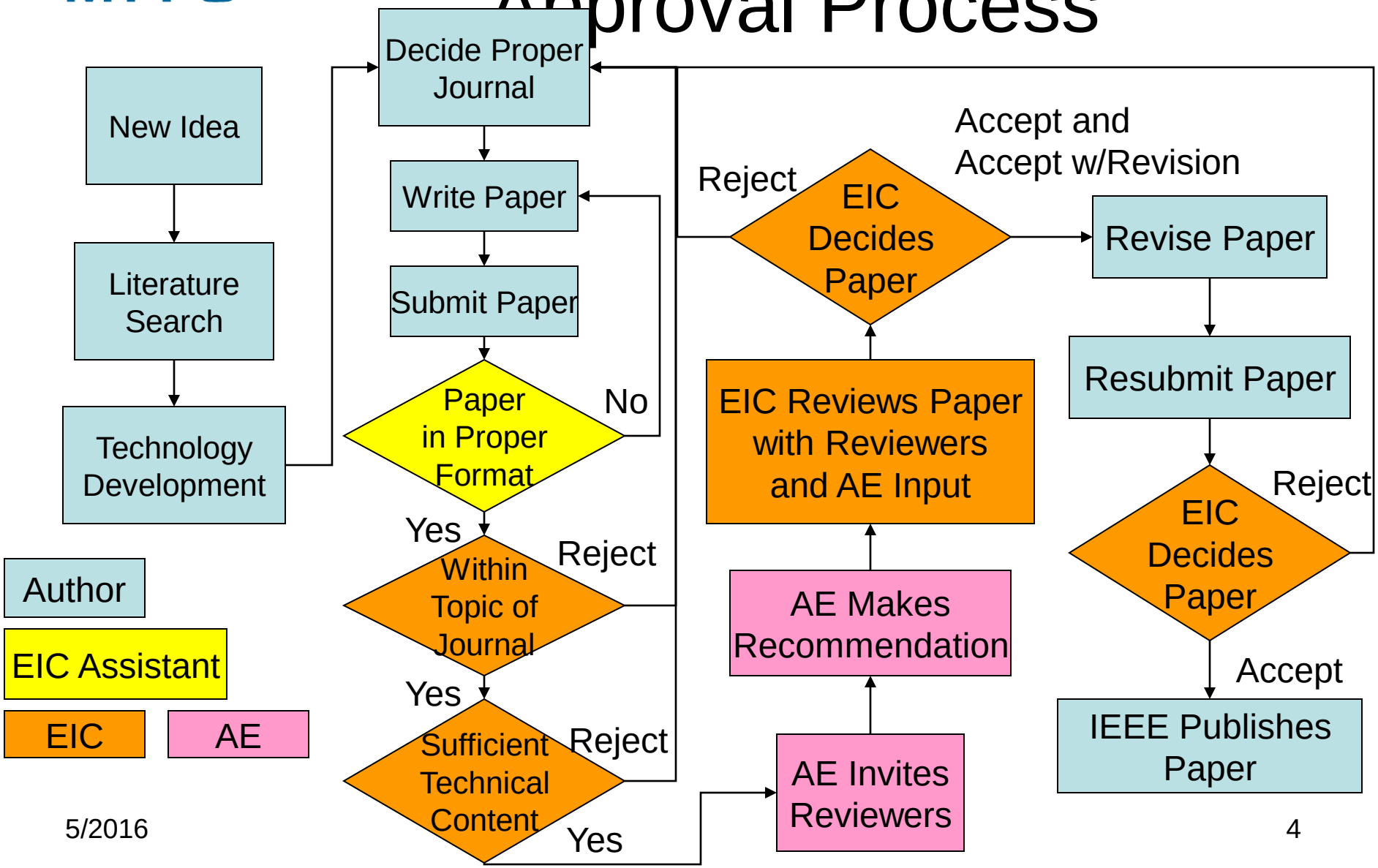
Science depends on the peer review process to assess paper technical correctness, novelty, significance!!

Conference Paper Writing / Approval Process



Note:
- No chance for revisions
- No chance to argue decision with an editor
- Often, you will not be told why your paper is accepted or rejected

Journal Paper Writing / Approval Process



Reasons for Rejection of Reviewed Papers

Note: Most reviewers look for reasons to reject a paper, not to accept it. Do not give them easy reasons.

1. Paper is very similar to another paper by the authors that was not referenced.
2. Idea not novel or it is an obvious, incremental variation over prior art.
3. Results are not significant.
4. Results are not state of the art.
5. Unsupported claims made in the paper.
6. Method or circuit are not fully explained.
7. Measured results not presented.
8. Poor grammar or use of English.

Reasons for Rejection

Not Referencing Prior Papers:

- Not referencing your own work that is similar almost always results in rejection. If you have published similar work, it is best to state so in the introduction and explain what is different in this paper.
- Be fair when referencing past work; reference work by all research groups.
- With IEEE Xplore and Google Scholar, the Editor or the reviewers will find prior papers by the authors.

Reasons for Rejection

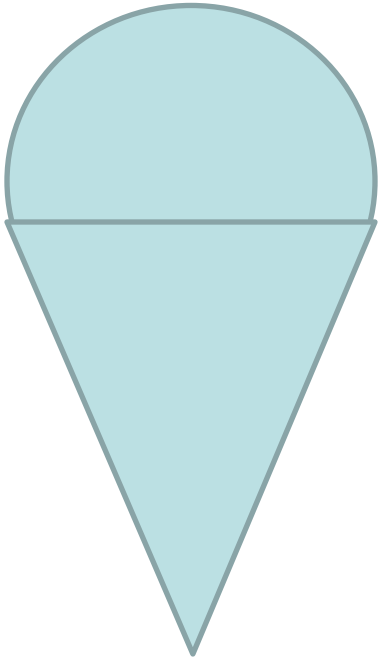
Low Novelty:

- IEEE publication rules require every paper to be new. There is no definition of how different a paper must be to be new. Generally, new material must be technical content, not more references and longer introduction.
- Paper is very similar to prior paper by other authors.
- Obvious, incremental variations of prior art are rejected.

Reasons for Rejection

Not Significant:

- Title: Development of numerical method that merges Cartesian and Circular coordinate systems for the solution of “Snowcone Waveguide”



The theory and numerical method may be very novel, but who is ever going to use “Snowcone Waveguide?” Who cares. Not Significant!!

Reasons for Rejection

Not State of the Art:

- IEEE does not publish papers that present “comparable” results.
- Reviewers are experts in their fields and expect new results to be better than prior results.

Reasons for Rejection

Unsupported Claims:

- Do not make any claims that are not supported by measurements, simulations, or comparisons to prior papers. Claims in the introduction of smaller, less memory required, less CPU time required, higher gain, etc. that are not supported will be rejected.

Reasons for Rejection

Method or circuits not Fully Explained:

- A practicing engineer must be able to duplicate your results based on your paper. Give all dimensions, important equations, materials, and circuit element values.
- Explain how the circuit works, and why the new circuit works better. Adding another circuit component to the model without explaining what it does and why will result in rejection. The reader must learn something!

Reasons for Rejection

Measured results not presented:

- The MWCL, the Trans. on Microwave Theory and Tech., the JSSC and many journals requires that all components and circuits be fabricated, a photo included, and measured results presented.
- Theory and numerical method papers require a comparison to another method.

Reasons for Rejection

Poor grammar or incorrect use of English:

- IEEE rules allow a paper to be rejected based solely on poor grammar.
- Most editors will try to help authors correct grammar errors.
- However, poor grammar makes the paper harder to read, so the reviewers are more likely to vote to reject the paper.

Writing the Paper

Write the paper to avoid easy rejections

Things NOT to do

- Plagiarism: All journal and most conference papers are run through computer programs to flag plagiarized papers.

Things NOT to do

- Paraphrasing: To avoid plagiarism computer checkers, authors have started paraphrasing prior papers. Changing another authors words but stealing their ideas is still plagiarism. In fact, because the author has tried to hide their crime, an IEEE committee often recommends more severe penalties.

Things NOT to do

- Presenting fake data or photos of circuits results in very severe punishments.

Things NOT to do

- Do not add citations to your previous papers that are NOT related to the topic of the current paper.

Things NOT to do

- Do not use AI to write your paper.

Things NOT to do

- If you are a reviewer, do not steal the authors ideas and try to publish them as your own.

Organization of Paper

- Title
- Abstract
- Introduction
- Technical Content
- Conclusions
- References

Organization of Paper

- Title and authors
- Abstract: 50 to 250 words that summarize the paper.
  - 1st to 3rd sentence tell what problem is being investigated.
  - How you performed the investigation.
  - Accomplishments and conclusions (summarize your results)

Abstract—Microwave and millimeter-wave integrated circuits and RF distribution networks often require two transmission lines to cross over each other. In this paper, experimental measurements and three-dimensional (3-D) finite difference time domain analysis are used to thoroughly characterize coplanar waveguide (CPW) and finite ground coplanar waveguide (FGC) 90-degree crossover junctions. It is shown that FGC crossover junctions have approximately 15 dB lower coupling than CPW crossover junctions. Furthermore, it is shown that the FGC junctions do not excite the parasitic slotline mode, whereas, the CPW junctions do excite the slotline mode. The results presented indicate that the FGC crossover junction is easier to implement and has better characteristics than the CPW crossover junction.

Index Terms—Coplanar waveguide, coupling, finite ground coplanar waveguide, planar transmission lines, transmission lines.

Organization of Paper

- Introduction (Hardest and most important part of paper, write this last)
  - 1st paragraph states problem to be solved and its importance
  - 2nd to nth paragraph states previous state of the art (Reference previous papers here, do not show bias towards or against any specific author or paper. Simply state the facts!)
  - Last paragraph states what is new in this paper (This statement is maybe the most important in the Introduction) and organization of the paper
- Many papers are rejected because of errors in the Introduction

Experimental Verification of the Use of Metal Filled Via Hole Fences for Crosstalk Control of Microstrip Lines in LTCC Packages

George E. Ponchak, *Senior Member, IEEE*, Donghoon Chun, Jong-Gwan Yook, *Member, IEEE*, and Linda P. B. Katehi, *Fellow, IEEE*

***Abstract*—Coupling between microstrip lines in dense RF packages is a common problem that degrades circuit performance. Prior three-dimensional-finite element method (3-D-FEM) electromagnetic simulations have shown that metal filled via hole fences between two adjacent microstrip lines actually increases coupling between the lines; however, if the top of the via posts are connected by a metal strip, coupling is reduced. In this paper, experimental verification of the 3-D-FEM simulations is demonstrated for commercially fabricated low temperature cofired ceramic (LTCC) packages. In addition, measured attenuation of microstrip lines surrounded by the shielding structures is presented and shows that shielding structures do not change the attenuation characteristics of the line.**

***Index Terms*—Coupling, crosstalk, microstrip, microwave transmission lines.**

I. Introduction

RF SYSTEMS being planned today integrate more functions in smaller packages that must cost less than those currently being used. Although several packaging technologies have been proposed to meet these goals [1]–[5], low temperature cofired ceramic (LTCC) may be the ideal packaging technology. The material used in LTCC has a moderate relative dielectric constant, ε_r, between four and eight, which permits wider microwave transmission lines and has lower conductor loss than circuits on Si, GaAs, and Alumina. It also has a low loss tangent of 0.002 at 10 GHz, which results in low dielectric attenuation. Packages are built with multiple layers of 0.1 to 0.15 mm thick ceramic layers with metal lines permitted on each layer and metal filled via holes interconnecting conductors on the different layers [2], [6]. Therefore, dense packages with RF integrated circuits, digital integrated circuits, bias lines, and interconnect lines may be built.

However, dense packages with closely spaced interconnect lines are prone to coupling or crosstalk that may severely degrade circuit performance. Microstrip transmission lines radiate at discontinuities [7], and this radiated power may couple to other microstrip lines. In addition, parallel microstrip lines couple energy to and from each other [8]. To help alleviate this coupling, metal filled via holes are often used to create Faraday cages that isolate sections of the package from each other [9]–[12]. Three-dimensional-finite element method (3-D-FEM) electromagnetic modeling of parallel microstrip lines separated by metal filled via hole fences has shown that the fences do not reduce coupling, but if the top of the via posts are connected with a metal strip, coupling is significantly reduced [13], [20], [14].

In this paper, commercial LTCC process and design layout rules are used to experimentally verify the 3-D-FEM electromagnetic modeling results. Test circuits are built by a commercial vendor and characterized over the frequency band of 2 to 40 GHz. First, the experimental procedures are presented. Then, coupling between parallel microstrip lines are presented as a function of frequency and the via fence geometry to verify the prior 3-D-FEM results [14]. Lastly, attenuation of the microstrip lines as a function of the via fence geometry is presented. Throughout the paper, the results are quantitatively and qualitatively compared to the 3-D-FEM results.

II. Circuit Fabrication and Design

Circuits are fabricated using commercial LTCC fabrication process and layout rules [15]. The ceramic material is mounted on a Cu/Mo/Cu metal core that is thermal coefficient of expansion (TCE) matched to the LTCC dielectric, Si, and GaAs. A single layer of ceramic tape is used for the microstrip substrate. This substrate is 0.005 in (127 μm) thick, has a relative dielectric constant, ε_r, of 5.67 at 12.5 GHz, and a volume resistivity of 5×10^{15} Ω-cm. According to the design rules, via holes are 0.008 in (203 μm) in diameter and have a minimum via to via spacing of 0.024 in (609 μm). All metal traces, including the microstrip lines, have a minimum conductor width and conductor-to-conductor line spacing of 0.008 in (203 μm). The metal filled vias and lines are Ag, with the lines coated with Ni/Au.

Microstrip lines are designed with a strip width, W, of 0.008 in (203 μm), which yields a theoretical characteristic impedance of 50 Ω. Referring to Fig. 1, microstrips with via to line spacing, S, of 0.012, 0.016, and 0.020 in (304, 406, and 508 μm) and via to via spacing, G, of 0.024 and 0.032 in

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Organization of Paper

- Body of paper separated into sections:
  1. Procedure (Design of the experiment)
  2. Results
  - Use clear figures and discuss all figures in the text
  - If paper is long, start each section with an introduction and end with a summary (few sentences)
- Summary or Conclusions (Emphasize what novel or good results were demonstrated. This is best done with a Table of Comparison or the use of Figure of Merit.)
- Acknowledgements (This can be added after acceptance of paper)

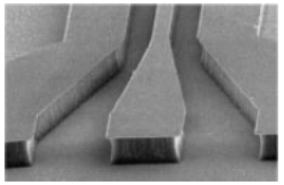

Fig. 2. SEM of micromachined CPW line on low-resistivity Si wafer with a polyimide interface layer ($Hp = 20.15$ μm) that has been etched.

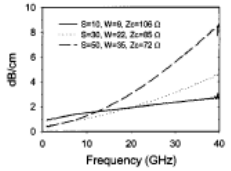

Fig. 3. Measured attenuation of micromachined CPW lines with $Hp = 20.15$ μm.

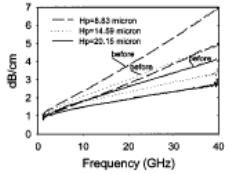

Fig. 4. Measured attenuation of CPW lines ($S = 10$ and $W = 9$ μm) before and after polyimide etch.

II. Fabrication and Test Procedures

On four 385-μm-thick 1-$\Omega \cdot$cm silicon wafers, DuPont WE 1111 (now called PI-1111) polyimide is deposited and cured to a thickness Hp of 6.35, 8.83, 14.59, and 20.15 μm. Sets of 15 different CPWs are fabricated on top of the polyimide using standard liftoff processing with the CPW made of 0.02 μm of Ti and 1.5 μm of Au. At this point, the transmission lines appear as shown in Fig. 1, where the polyimide not protected by the CPW metallization is removed by reactive ion etching (RIE) to obtain the structure shown in Fig. 2. No backside ground plane or Si passivation layers are grown, and WE1111 polyimide has a relative dielectric constant ε_{r1} of 2.8.

The CPW propagation characteristics are measured with a vector network analyzer and probe station. A quartz spacer between the Si substrate and the probe station wafer chuck is used to eliminate parasitic microstrip and parallel-plate waveguide modes. The propagation constant $\gamma = \alpha + j\omega\sqrt{\varepsilon_{\text{eff}}}/c$, where α is the attenuation constant, ω is the angular frequency, c is the velocity of light in vacuum, and ε_{eff} is the effective dielectric constant, is deembedded through the thru-reflect-line (TRL) calibration routine implemented in the software program MULTICAL [11]. For each CPW line characterized, four delay lines with the longest line being 1 cm are used in addition to the thru line to enhance accuracy from 1 to 40 GHz.

The micromachined CPW lines are theoretically analyzed using a 3-D-FEM analysis implemented through Ansoft's high-frequency structure simulator (HFSS). The simulated structure is the same as the actual structure described above and is shown in Fig. 2, including the 2-μm polyimide undercut of the CPW lines. Furthermore, to achieve good match between the measured and theoretical results, the Si wafer loss tangent of 0.0018 [12], the Si wafer resistivity, and the metal resistivity were used in the model. Radiation boundaries are used on the top and sides of the simulated structure.

III. Results

The attenuation in decibels per centimeter of three CPW lines after polyimide etch with $Hp = 20.15$ μm is shown in Fig. 3. At low frequency, below X-band, wider CPW lines have lower loss than narrow lines; however, the high-frequency behavior is not easily predicted. It is seen in Fig. 3 that the frequency dependence n of $\alpha = af^n$ varies with the strip and slot widths. Specifically, for narrow lines, the attenuation is conductor-loss dominated and varies as $f^{0.5}$, while for wider lines, the frequency dependence n increases to 1.5. Therefore, at high frequency, narrower CPW lines on polyimide have lower attenuation than wider lines. This is contrary to the attenuation characteristics of CPW lines on insulating substrates, which are dominated by conductor loss for both narrow and wide lines [13]. Note that, in Fig. 3, the lowest attenuation at 40 GHz is 2.75 dB/cm for a line with S and W of 10 and 9 μm, respectively.

Fig. 4 shows the reduction in attenuation after etching the polyimide from the slots of three CPW lines with S and W of 10 and 9 μm, respectively, on polyimide of thickness 8.83, 14.59, and 20.15 μm. Note that each graph on Fig. 4 is for a different polyimide thickness and the upper line, indicating higher loss, is the attenuation of the CPW before polyimide etch. At 40 GHz, there is a 28% reduction in attenuation after etching for the CPW on the thinnest polyimide and a 35% reduction in attenuation for the CPW on the thickest polyimide. It is interesting that this reduction in attenuation is similar to the reduction in attenuation of CPW lines on HRS when the silicon is etched from the slots [9], [10].

The effective permittivity of the CPW lines after etching the polyimide also varies with the line geometry. If the approximate, but usually very accurate, estimate of $\varepsilon_{\text{eff}} = (\varepsilon_r + 1)/2$ is used, ε_{eff} should equal 1.9 for the CPW lines before the polyimide is etched if none of the fields interact with the silicon since $\varepsilon_r = \varepsilon_{r1} = 2.8$. Furthermore, the more the electric fields interact with the Si substrate, the higher ε_{eff} will be. After the polyimide is etched and more of the fields are in air, both above the polyimide and in the slot region, ε_{eff} should to be less than 1.9. Fig. 5 shows the measured and calculated ε_{eff} as a function of frequency for a narrow and a wide CPW line before and after the polyimide etch. There is excellent agreement between the

References

References should:

- Put paper in context with prior work. If reporting a state of the art result, references should be used for comparison. Newer references with the latest results are preferred to older references.
- Provide supplemental information. There is no need to repeat well known ideas, equations, or facts in your paper.

Helpful Hint: At least some of the references should come from the journal that you are submitting to. This shows that the paper is within the topic of the journal. Also, some journals with unethical editors use this as a method of increasing their Impact Factor.

Before Submission

- Have all co-authors read the paper and make revisions.
- Have a non-author read the paper for clarity. After spending several weeks writing the paper, you tend to overlook obvious errors.
- Submit required government and company forms.

Submit Papers

- Visit submission web site http://www.mtt.org/publications/index.htm and follow procedures.

Letter from Editor after Review

Dear Dr. George Ponchak:

Your manuscript entitled, Coupling Between Microstrip Lines With Finite Width Ground Plane Embedded in Thin Film Circuits, by Dr. George Ponchak, et. al., is rejected in its current form. We ask you to revise your manuscript in response to the Associate Editor's/reviewers' comments which are at the end of this letter.

Thank you for submitting your paper to the IEEE Transactions on Advanced Packaging.

Sincerely yours,

This is a good review. It is very rare that a paper is accepted without reviewers comments that need to be addressed. Read all reviews and address each comment. Note that reviewers comments are meant to help you strengthen your paper. If the reviewers did not like your paper, they would state this to the editor in a separate letter.

Reviewers Comments

This paper investigates the modes that occur in multilayer MCM-D structures when the grounds of two microstrip lines are not connected. The conclusion is that the two lines perform better (less coupling) when the grounds are connected than they do if the grounds are not connected. This is not much of a surprise.

Additional comments.
- The field plots are interesting
- The possibility of a dielectric mode is interesting, but there needs to be more investigation of it. Presumably the dielectric mode is related to a lossy mode in the low resistivity silicon.
- There needs to be more explanation of how Eeff is extracted for the various modes.
- At the beginning of Section 5, the increasing attenuation of W2 is blamed on radiation. This seems unlikely for the small size of the structure, and with no resonances. More likely is that the W2 mode is extending its currents into the low resistivity Silicon. Thus the loss increases.

Author's Reply with Resubmission

Write a polite response to each point that the reviewers identified. Include a description of how you revised the paper to improve it based on the reviewers' comments.

- "At the beginning of Section 5, the increasing attenuation of W2 is blamed on radiation. This seems unlikely for the small size of the structure, and with no resonances. More likely is that the W2 mode is extending its currents into the low resistivity Silicon. Thus the loss increases."
- Response: The authors appreciated your comments and we reexamined the field plots. We deleted our previous assumption on why the loss increased and added "FDTD simulations show that the magnitude of the electric fields excited into the silicon wafer from the edges of the ground planes increases with frequency. Furthermore, microstrip lines with thicker substrates, such as W2, have greater excitation of electric fields in the silicon than lines on thinner substrates. Therefore, since the silicon is a lossy substrate, this is probably the reason for higher loss for line W2 at higher frequency."
- In the revised paper, highlight all revisions.

If Paper is Rejected

- IEEE Transactions and Letters reject between 80 and 50 % of papers submitted. Do not take it personal.
- If your paper is rejected, read all of the reviewers' comments. The reviewers and the editors are experts in the field and the comments should help strengthen the paper.
- Revise your paper to address all of the relevant comments. Note that reviewers often review for many journals. If they are the expert in the field of your paper, they may be asked to review it again, even if submitted to a different journal. In revised paper, highlight all revisions made.
- If invited to resubmit the paper by the editor, then resubmit the revised paper within 1 to two months.
- If editor does not invite resubmission, I suggest selecting a different journal or sending the editor a letter asking if a resubmission would be welcome. IEEE allows for resubmitted papers, but the editor does not have to send them for review if the paper was not revised.